Muhammad Farhan Azmine

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Education

Virginia Tech (GPA: 4.00 / 4.00) *Blacksburg & Alexandria, VA*
PhD in Computer Engineering (Direct PhD; MS completed) *Aug 2022 – May 2027 (Expected)*

Bangladesh University of Engineering and Technology (BUET) *Dhaka, Bangladesh*
Bachelors of Science in Electrical & Electronics Engineering *Jan 2013 – Sep 2017*

- **Relevant Coursework:** Digital Design II, Testing VLSI Techniques, Advanced Computer Architecture, VLSI Device Modeling, Advanced Analog IC Design, Deep Learning, Advanced Machine Learning, Computation in Data Science

Publications

- **Muhammad F. A.**, Li, R., Sharma, G., & Yi, Y. (2025). SpikeSpec: On-Chip Learning Neuromorphic Accelerator for Spectrum Sensing. *IEEE Transaction CAD*, Feb 2025.
- Li, R., **Muhammad F. A.**, Sharma, G., & Yi, Y. (2025). Efficient Digital Architecture of Spiking Encoders. In *Proc. ISQED 2025*.
- Lin, C., **Muhammad F. A.**, Liang, Y., & Yi, Y. (2024). Neuro-Inspired AI Accelerator for 6G Networks. *Front. Comput. Neurosci.*
- Lin, C., **Muhammad F. A.**, & Yi, Y. (2023). Accelerating Wireless Communications with FPGA-Based AI. In *ICCAD 2023*.

Recent- Tapeout

- Taped out a RV32I RISC-V CPU on Sky130 PDK (21.8K cells, 334.9K µm², 15.9 mW), with full ISA verif. & post-layout validation.

Research & Design Experience

Research Assistant *(Functioning as RTL Engineer – Complex Digital System Design & Verification)* *June 2023 – present*
Supervisor : Dr. Yang (Cindy) Yi

DSP48E1 IP based RTL chip implementation of energy efficient On-Chip training RNN network in ZCU104 FPGA
Summer 24-Spring 25

- Achieved **100% SystemVerilog design validation** through **Vivado IP integrator** on Zynq SoC, enabling real-time sample delivery to **RTL (PL)** and result capture via **ZynQ AXI-UART (PS)** , with a **custom C++ parser through Vitis** for CSV input processing and output generation.
- **Decreased dynamic power consumption by 65%** by replacing CLB-based matrix adder-multiplier with a pipelined **DSP48 adder tree** for MAC operations, resulting in 86% LUT and 64% FF utilization reduction.
- **Cut wire delay by 3.2ns** through **fanout optimization** to boost operating frequency.

SerDes based Spiking Neural Network RTL design with On-Chip learning for Spectrum-Sensing in Virtex-707 FPGA
[Github link] *Fall 22 - Spr 24*

- Designed and implemented a custom **SerDes driver** featuring an **8b/10b encoder and 10b/8b decoder** to transfer data over **GTX** pins, facilitating direct PL access and reducing overall **FPGA I/O pin count** through **Vivado Constraints Wizard**.
- Reduced **RTL area by 60% in SystemVerilog** using resource-shared **adders and LUTs** via **serialization with SIPO shift registers**.
- **Throughput increase** by **58 MHz** with critical path balancing between **priority encoder & exponential approximator**
- **Reduced latency** by **50%** using simple **dual port memory ram** in read-then-write mode for weight learning update
- Improved performance accuracy **by 3.88%** through **priority encoder and fixed-point exponential approximator** for weight update engine

RTL integration of Ethernet-MAC IP with AI Accelerator inference chip for symbol detection in Virtex-709 FPGA
[Github link] *Spring 23-Fall 23*

- **Improved SystemVerilog verification coverage by 30%** through modifying BIST testbench in frame data transfer between Ethernet-PHY and target accelerator by creating **over 4 protocol-variant Ethernet frame stimulus patterns** including error-injection & backpressure scenarios
- **Boosted design frequency by 100 MHz** by implementing **Clock Domain Crossing** to achieve 200 MHz frequency for target accelerator through synchronizing with Ethernet PHY communication at 125 MHz using **Ping-pong buffer, CDC AXI-handshake IPs and Asynchronous FIFOs**
- **Increased data transfer throughput 5x** by Ethernet-MAC IP integration with target accelerator design at 125 MHz frequency
- **Performed 100% ML algorithm verification** using **C++ simulator** $\langle 16, 10 \rangle$ fixed-point format with template libraries like **std::vector**
- **Reduced IP area usage in SystemVerilog RTL by 33.3%** through **DSP48E1 IP** integration at RTL-level for inference MAC operation

Technical Skills

- **Techniques:** RTL design, STA, Power optimization, Clock-Domain-Crossing, UVM, DFT, FPGA-IP Integration, ASIC implementation
- **Languages:** SystemVerilog, Verilog, VHDL, Matlab (Script), Python (OOP) [Github link], C++, Java [Github link], Tcl, Linux Shell
- **Tools:** Cadence Suite (Xcelium, Genus & JasperGold), TensorFlow [Github link], PyTorch, Scikit-learn [Github link] , Vivado, Quartus
- **Concepts:** UVM, SVA Formal Verification, AXI-DMA, AXI4, UART, Ethernet-TCP/UDP, SPI, VGA, RISC V ISA, Cache memory mapping