Muhammad Farhan Azmine

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Education

Virginia Tech (GPA: 4.00 / 4.00) *Blacksburg & Alexandria, VA*
PhD in Computer Engineering (Direct PhD; MS completed) *Aug 2022 – May 2027 (Expected)*

Bangladesh University of Engineering and Technology (BUET) *Dhaka, Bangladesh*
Bachelors of Science in Electrical & Electronics Engineering *Jan 2013 – Sep 2017*

- **Relevant Coursework: Deep Learning, Advanced Machine Learning, Advanced Digital Design,** Advanced Computer Architecture, Testing VLSI Techniques, VLSI Device Modeling, Advanced Analog IC Design, Computation in Data Science

Research & Design Experience

Research Assistant *(Functioning as RTL Engineer – Complex Digital System Design & Verification)* *June 2023 – present*
Supervisor : Dr. Yang (Cindy) Yi

TensorFlow Transfer Learning (VGG16 Encoder) & U-Net Segmentation for Road Extraction from Satellite Imagery
[Github link] *Spring 2024*

- Built a **TensorFlow/Keras road-extraction pipeline** using **U-Net** and **VGG16-encoder** for satellite image segmentation on the **DeepGlobe** dataset.
- Preprocessed DeepGlobe Satellite images in **Python** using **OpenCV (cv2)**, **NumPy**, and **Pandas** by **resizing 1024×1024 to 256×256** and **binarizing masks at 128** for pixel-wise segmentation.
- Achieved best performance with **U-Net + Nadam**: **96.7% training IoU** and **96.5% validation IoU**; **U-Net + Adam** reached **95.6%/95.4% IoU** (train/val).
- Benchmarked **VGG16-UNet** with early stopping at 4 epochs, delivering **69.6% training IoU** and **68.09% validation IoU** to quantify transfer-learning tradeoffs.
- Compared additional baselines: **SEG-net** reached **59.0% validation IoU**, while **CNN+XGBoost** examples achieved image-wise IoU up to **42%**, highlighting performance gaps.

Automatic Seizure Detection on MIT & Siena EEG after feature extraction & selection with Lightweight ML Ensembles
[Github link] *Spring 2023*

- Built a real-time AI pipeline for EEG seizure detection across **4,744 samples from 36 patients**, achieving up to **99.5% accuracy** and $>$**98% sensitivity** on external data from MIT & Siena datasets.
- Engineered diverse EEG features (time, frequency, and statistical), and used **feature selection** (Joint Mutual Information (JMI) and Minimum Redundancy Maximum Relevance (MRMR)) to **reduce input data by 95%**.
- Experimented with and optimized diverse ML models, including **LogisticRegression**, **DecisionTree**, **MLPClassifier**, and lightweight ensemble methods (**VotingClassifier**, **RandomForestClassifier**, **XGBoost**) for peak performance.
- Applied unsupervised learning (**KMeans** with custom Condensed Silhouette Score) to analyze clustering structure of seizures. Tuned all models using **grid search**, **cross-validation**, and **confusion matrix** metrics.
- Leveraged **Python** (**pandas**, **numpy**, **scikit-learn**, **mifs**, **mrmr**), **MATLAB** (data segmentation), and custom **Python** scripts for a fully automated, scalable, cloud-adaptable workflow.

A Hardware Friendly Artificial Neural Network inference chip design for OFDM symbol detection
[Github link] *Spring 23-Fall 23*

- **Performed 100% ML algorithm verification** using **C++ simulator** $\langle 16, 10 \rangle$ fixed-point format with template libraries like **std::vector**
- **Reduced IP area usage in SystemVerilog RTL by 33.3%** through **DSP48E1 IP** integration at RTL-level for **ANN inference MAC operation**
- **Boosted design frequency by 100 MHz** by implementing **Clock Domain Crossing** to achieve 200 MHz frequency for target accelerator through synchronizing with Ethernet PHY communication at 125 MHz using **Ping-pong buffer, CDC AXI-handshake IPs and Asynchronous FIFOs**
- **Improved SystemVerilog verification coverage by 30%** through modifying BIST testbench in frame data transfer between Ethernet-PHY and target accelerator by creating **over 4 protocol-variant Ethernet frame stimulus patterns** including error-injection & backpressure scenarios
- **Increased data transfer throughput 5x** by Ethernet-MAC IP integration with target accelerator design at 125 MHz frequency

Technical Skills

- **SSD/SoC Concepts:** AXI/AXI4, DMA, Cache Memory Mapping [Github link], Clock Domain Crossing (CDC), RTL Design, DFT, STA, PPA [Github link], UVM, SVA, Scoreboard, Coverage Analysis [Github link], Constrained Random Stimulus, FPGA/ASIC Implementation [Github link]
- **AI/ML Concepts:** **[Github link]** Neural Networks (MLP, CNN, U-Net, VGG16), Random Forest, Decision Tree, Logistic Regression, Clustering (KMeans), Feature Selection (MRMR, JMI), Cross-Validation, Confusion Matrix, Hyperparameter Tuning (GridSearchCV), Data Preprocessing (Imputation, Scaling)
- **Languages:** Python (OOP, Data Science, ML) [Github link], Java [Github link], C++, SystemVerilog, Verilog, Matlab (Script), SQL, Tcl, Bash
- **Frameworks & Tools:** TensorFlow [Github link], PyTorch, Scikit-learn [Github link], XGBoost, pandas, numpy, matplotlib, Docker, Kubernetes, Git, Jupyter, Cadence Suite (Xcelium, Genus, JasperGold), Vivado, Quartus